CLAIMS

What is claimed is:

1. A method of mapping logic failures in an integrated circuit die comprising steps of:

(a) generating a navigation map of test paths for an integrated circuit die;

(b) selecting a grid spacing to define a grid map of cell locations from the navigation map for each of the test paths; and

(c) calculating a value for each of the cell locations wherein the value is representative of the difference between a total number of the test paths intersecting each of the cell locations and a failed number of the test paths intersecting each of the cell locations.

2. The method of Claim 1 wherein step (b) further comprises selecting the grid spacing so that a probability of multiple random defects occurring in an identical one of the cell locations is less than a selected threshold.

3. The method of Claim 1 wherein step (b) further comprises a step of selecting the grid spacing of 50 to 200 microns.

4. The method of Claim 1 wherein step (c) further comprises assigning a first value to each cell location in a grid map that is intersected by one of the test paths and assigning a second value to each cell location in the grid map that is not intersected by one of the test paths to define a grid matrix for each grid map.

5. The method of Claim 4 wherein step (c) further comprises generating a first combined grid matrix equal to a sum of the grid matrix for each of the total number of the test paths.

6. The method of Claim 4 wherein step (c) further comprises generating a second combined grid matrix equal to a sum of the grid map for each of the failed number of the test paths.

7. The method of Claim 6 wherein step (c) further comprises generating a third combined grid matrix representative of a difference between the first combined grid matrix and the second combined grid matrix.

8. The method of Claim 7 wherein step (c) further comprises dividing each element of the third combined grid matrix by the total number of the test paths.

9. The method of Claim 1 further comprising filtering the value for each of the cell locations to remove values for the cell locations that contain a number of logic failures below a selected threshold to generate a filtered comparison matrix.

10. The method of Claim 9 further comprising displaying the filtered comparison matrix to identify the cell locations of logic failures that are related to a common physical feature of the integrated circuit die.

11. A computer program product for mapping logic failures in an integrated circuit die comprising:

a medium for embodying a computer program for input to a computer; and

a computer program embodied in the medium for causing the computer to perform steps of:

(a) generating a navigation map of test paths for an integrated circuit die;

(b) selecting a grid spacing to define a grid map of cell locations from the navigation map for each of the test paths; and

(c) calculating a value for each of the cell locations wherein the value is representative of the difference between a total number of the test paths intersecting each of the cell locations and a failed number of the test paths intersecting each of the cell locations.

12. The computer program product of Claim 10 wherein step (b) further comprises selecting the grid spacing so that a probability of multiple random defects occurring at an identical one of the cell locations is less than a selected threshold.

13. The computer program product of Claim 10 wherein step (b) further comprises a step of selecting the grid spacing of 50 to 200 microns.

14. The computer program product of Claim 10 wherein step (c) further comprises assigning a first value to each cell location in each grid map that is intersected by one of the test paths and assigning a second value to each of the cell locations in each grid map that is not intersected by one of the test paths to define a grid matrix for each grid map.

15. The computer program product of Claim 14 wherein step (c) further comprises generating a first combined grid matrix equal to a sum of the grid map for each of the test paths.

16. The computer program product of Claim 15 wherein step (c) further comprises generating a second combined grid matrix equal to a sum of the grid map for each of the failed number of the test paths.

17. The computer program product of Claim 16 wherein step (c) further comprises generating a third combined grid matrix representative of a difference between the first combined grid matrix and the second combined grid matrix.

18. The computer program product of Claim 17 wherein step (c) further comprises dividing each element of the third combined grid matrix by the total number of the test paths.

19. The computer program product of Claim 10 further comprising filtering the value for each of the cell locations to remove values for the cell locations that contain a number of logic failures below a selected threshold to generate a filtered comparison matrix.

20. The computer program product of Claim 19 further comprising displaying the filtered comparison matrix to identify the cell locations of logic failures that are related to a common physical feature of the integrated circuit die.